AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An analog front-end having built-in equalization, the analog front-end comprises:

control module operably coupled to provide a frequency response setting based on a channel response of a channel providing high-speed serial data to the analog front end; and

tunable gain stage operably coupled to amplify and equalize the high-speed serial data based on the frequency response setting, wherein the tunable gain stage ~~includes~~ comprises:

a frequency dependent load that is adjusted based on the frequency response setting; [[and]]

amplifier input section operably coupled to the frequency dependent load, wherein the amplifier input section receives the high-speed serial data and, in conjunction with the frequency dependent load amplifies and equalizes the high-speed serial data to produce an amplified and equalized serial data; .

a first stage operably coupled to amplify and equalize, to a first level, the high-speed serial data based on the frequency response setting to produce a first amplified and equalized serial data; and

a second stage operably coupled to amplify and equalize the first amplified and equalized serial data based on the frequency response setting to produce the amplified and equalized serial data, the second stage comprising:

an input stage operably coupled to amplify and equalize the first amplified and equalized serial data based on the frequency response setting to produce intermediate amplified and equalized serial data; and

an output stage operably coupled to amplify and equalize the intermediate amplified and equalized serial data based on the frequency response setting to produce the amplified and equalized serial data

Claims 2. and 3. (Cancelled)

4. (Original) The analog front-end of claim 1, wherein the frequency dependent load further comprises at least one high pass filter.

5. (Original) The analog front-end of claim 4, wherein each of the at least one high pass filter further comprises:

a transistor having a gate, a drain, and a source;

an adjustable resistor operably coupled to the gate and the drain of the transistor, wherein a resistance value of the adjustable resistor is set based on the frequency response setting, and wherein parasitic capacitance of the transistor and the adjustable resistor establish a corner frequency for the each of the at least one high pass filter.

6. (Original) The analog front-end of claim 5, wherein the each of the at least one high pass filter further comprises:

a capacitor operably coupled between the gate and source of the transistor, wherein the capacitor, the parasitic capacitance and the adjustable resistor establish the corner frequency for the each of the at least one high pass filter.

7. (Original) The analog front-end of claim 1, wherein the tunable gain stage further comprises:

the frequency dependent load including:

a transistor having a gate, a drain, and a source;

an adjustable resistor operably coupled to the gate and the drain of the transistor, wherein a resistance value of the adjustable resistor is set based on the frequency response setting;

the amplifier input section including:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive, as a single-ended signal, the high-speed serial data, and the drain of the input transistor is operably coupled to the source of the transistor to provide the amplified and equalized serial data; and

current source operably coupled to the source of the input transistor and to a voltage return.

8. (Original) The analog front-end of claim 1, wherein the tunable gain stage further comprises:

the frequency dependent load including:

a first transistor having a gate, a drain, and a source;

a first adjustable resistor operably coupled to the gate and the drain of the first transistor, wherein a resistance value of the first adjustable resistor is set based on the frequency response setting;

a second transistor having a gate, a drain, and a source;

a second adjustable resistor operably coupled to the gate and the drain of the second transistor, wherein a resistance value of the second adjustable resistor is set based on the frequency response setting;

the amplifier input section including:

a first input transistor having a gate, a drain, and a source, wherein the gate of the first input transistor is operably coupled to receive, as one leg of a differential signal, the high-speed serial data, and the drain of the first input transistor is operably coupled to the source of the first transistor to provide one leg of the amplified and equalized serial data;

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor is operably coupled to receive, as another leg of a differential signal, the high-speed serial data, and the drain of the second input transistor is operably coupled to the source of the second transistor to provide another leg of the amplified and equalized serial data;

current source operably coupled to the sources of the first and second input transistors and to a voltage return.

Claims 9.-15. (Cancelled)

16. (Currently Amended) A high-speed data receiver comprises:

an analog front-end operably coupled to amplify and equalize high-speed data to produce amplified and equalized high-speed data; and

a clock and data recovery module operably coupled to recover a clock signal and data from the amplified and equalized high-speed data, wherein the analog front-

end includes:

a control module operably coupled to provide a frequency response setting based on a channel response of a channel providing the high-speed data to the analog front end; and

a tunable gain stage operably coupled to amplify and equalize the high-speed data based on the frequency response setting, wherein the tunable gain stage includes:

a frequency dependent load that is adjusted based on the frequency response setting and comprises at least one high pass filter, the at least one high pass filter comprising:

a transistor having a gate, a drain, and a source; and

an adjustable resistor operably coupled to the gate and the drain of the transistor, wherein a resistance value of the adjustable resistor is set based on the frequency response setting, and wherein parasitic capacitance of the transistor and the adjustable resistor establish a corner frequency for the each of the at least one high pass filter; and

an amplifier input section operably coupled to the frequency dependent load, wherein the amplifier input section receives the high-speed data and, in conjunction with the frequency dependent load amplifies and equalizes the high-speed data to produce an amplified and equalized serial data.

17. (Original) The high-speed data receiver of claim 16, wherein the tunable gain stage further comprises:

a first stage operably coupled to amplify and equalize, to a first level, the high-speed data based on the frequency response setting to produce a first amplified and equalized serial data; and

a second stage operably coupled to amplify and equalize the first amplified and equalized serial data based on the frequency response setting to produce the amplified and equalized serial data.

18. (Original) The high-speed data receiver of claim 17, wherein the second stage further comprises:

an input stage operably coupled to amplify and equalize the first amplified and equalized serial data based on the frequency response setting to produce intermediate amplified and equalized serial data; and

an output stage operably coupled to amplify and equalize the intermediate amplified and equalized serial data based on the frequency response setting to produce the amplified and equalized serial data.

Claims 19. and 20. (Cancelled)

21. (Currently Amended) The high-speed data receiver of claim[[20]] 16, wherein the each of the at least one high pass filter further comprises:

a capacitor operably coupled between the gate and source of the transistor, wherein the capacitor, the parasitic capacitance and the adjustable resistor establish the corner frequency for the each of the at least one high pass filter.

22. (Original) The high-speed data receiver of claim 16, wherein the tunable gain stage further comprises:

the frequency dependent load including:

a transistor having a gate, a drain, and a source;

an adjustable resistor operably coupled to the gate and the drain of the transistor, wherein a resistance value of the adjustable resistor is set based on the frequency response setting;

the amplifier input section including:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive, as a single-ended signal, the high-speed data, and the drain of the input transistor is operably coupled to the source of the transistor to provide the amplified and equalized serial data; and

current source operably coupled to the source of the input transistor and to a voltage return.

23. (Original) The high-speed data receiver of claim 16, wherein the tunable gain stage further comprises:

the frequency dependent load including:

a first transistor having a gate, a drain, and a source;

a first adjustable resistor operably coupled to the gate and the drain of the first transistor, wherein a resistance value of the first adjustable resistor is set based on the frequency response setting;

a second transistor having a gate, a drain, and a source;

a second adjustable resistor operably coupled to the gate and the drain of the second transistor, wherein a resistance value of the second adjustable resistor is set based on the frequency response setting;

the amplifier input section including:

a first input transistor having a gate, a drain, and a source, wherein the gate of the first input transistor is operably coupled to receive, as one leg of a differential signal, the high-speed data, and the drain of the first input transistor is operably coupled to the source of the first transistor to provide one leg of the amplified and equalized serial data;

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor is operably coupled to receive, as another leg of a differential signal, the high-speed data, and the drain of the second input transistor is operably coupled to the source of the second transistor to provide another leg of the amplified and equalized serial data;

current source operably coupled to the sources of the first and second input transistors and to a voltage return.

Claims 24.- 30. (Cancelled)